
Winchester

Winchester

Contents

1 Assembly and Disassembly

1 Assembly And Disassembly

1. General Recommendation

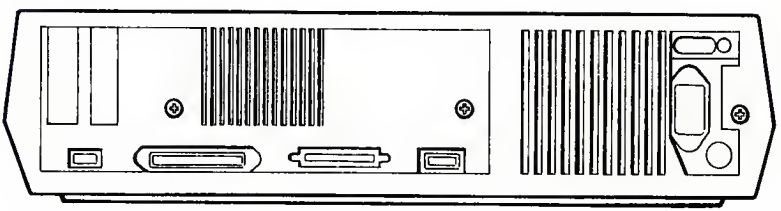
1. Disconnect from mains supply before disassembling machine.
2. Unless specifically noted, assembly is the reverse of Disassembly and will not be described unless necessary.
3. Do not mix screws (length, diameter)
4. A number in parenthesis thus (4) indicates the number of screws to be slakened or removed to remove that particular part.

   Warning -

   When bench testing or working on a drive, a foam mat should be placed underneath the unit to reduce the risk of accidental damage if the drive is dropped or topples over. It is recommended that a PVC skinned foam sheet approximately one inch thick is used.

   Engineers are reminded that the Winchester module is a sealed unit. Removal of the module cover will render any returns void.

2 Rear panel and top cover

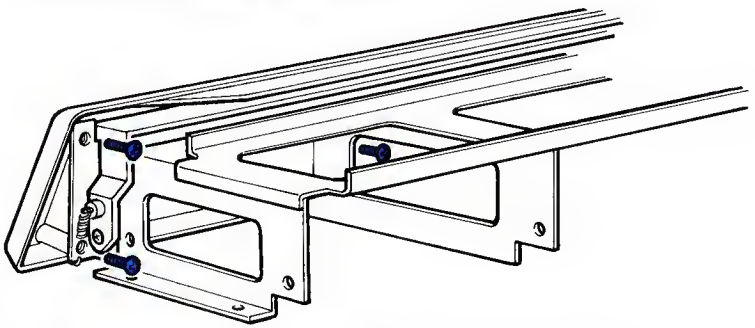


1. Remove M4 X 12mm screws (3).
2. Allow rear panel to tilt backwards and remove top cover by lifting at rear slightly and disengaging lip from front bezel.
3. Remove A.C input connector on P.S.U and all earth leads.

Assembly

Reverse of above procedure.

3. Chasis Bridge Assembly

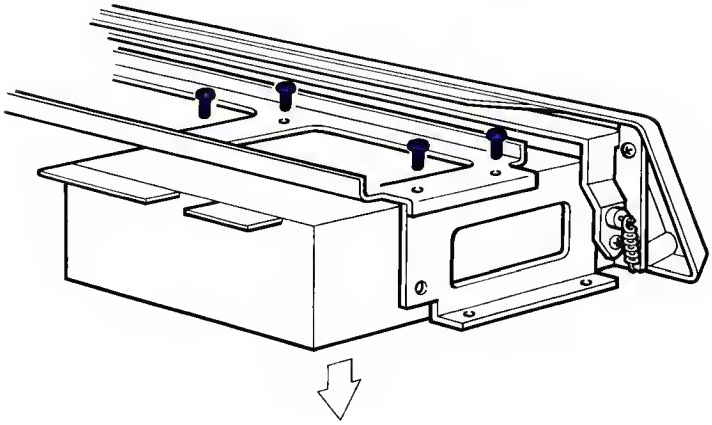


1. Remove rear panel and top cover as in Section 1.
2. Disconnect power and ribbon cables from disk drives.
3. Slaken M3 x 6mm screws (4)
4. Lift chassis bridge assembly away from the main chasis.

Assembly

Reverse of above procedure.

4. Winchester Disk Drive



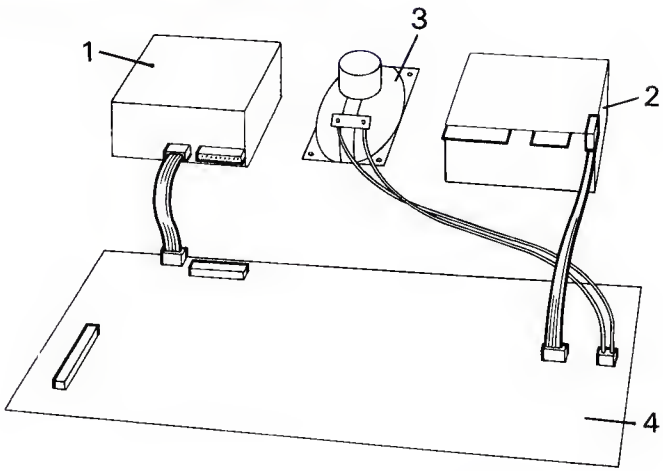
1. Remove chassis bridge assembly as in Section II
2. Remove 9 x 36 unc screws (4)
3. Slide Winchester drive out.

Assembly

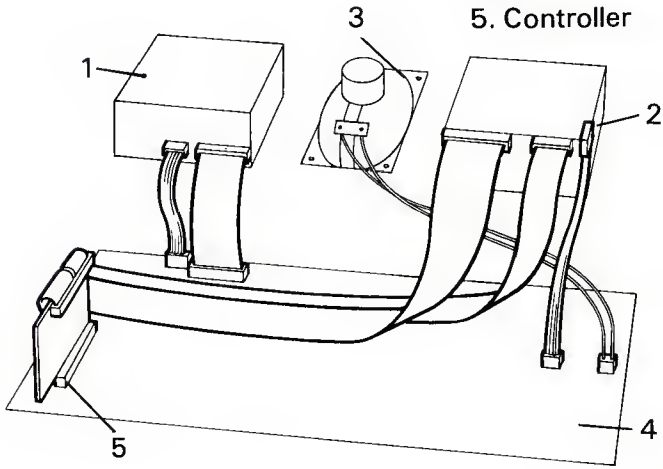
Reverse of above procedure.

1. Interconnection Diagram
2. Connector Pin-Outs

1. Interconnection Diagram



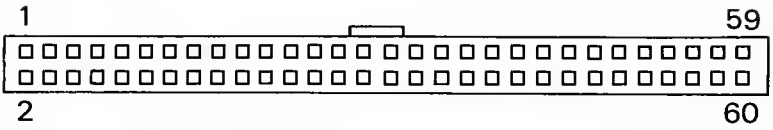
1. Floppy Drive
2. Winchester Drive
3. Loud Speaker
4. PCB
5. Controller



2. Connector Pin-Outs.

Winchester Cable Controller End

↓ Red strip denotes pin 1.



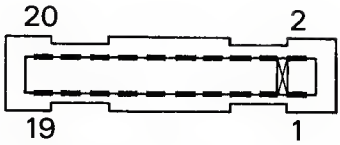
2	RWC	28	Drive Select 2
4	Head Select 2	30	Drive Select 3
6	Write Gate	32	Drive Select 4
8	Seek Complete	34	Dir
10	Track 00	36	
12	Write Fault	38	
14	Head Select 0	40	
16		42	
18	Head Select 1	44	
20	Index	47	+MWD
22	Ready	48	—MWD
24	Step	51	+MRD
26	Drive Select 1	52	—MRD
		54	

1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 36, 38, 40, 42, 45, 46, 49, 50, 53, 54 Ground returns.

55-60 not used

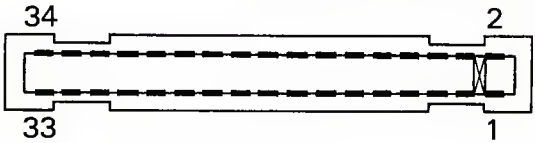
Winchester Cable Drive End

Data Interface



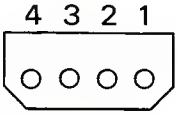
GND	Signal Pin	Signal Name
2	1	Drive Selected
4	3	Reserved
6	5	Spare
8	7	Reserved
10	9	Spare
	11	GND
	13	+MFM write data
	14	—MFM write data
16	15	GND
	17	+MFM read data
	18	—MFM read data
20	19	GND

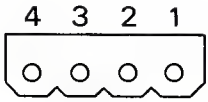
Winchester Cable Drive End Control Interface



GND Pin	Signal Pin	Signal Name
1	2	Reserved
3	4	Reserved
5	6	Write gate
7	8	Seek complete
9	10	Track 0
11	12	Write fault
13	14	Head select 0
15	16	Reserved
17	18	Head select 1
19	20	Index
21	22	Ready
23	24	Step
25	26	Drive Select 1
27	28	Drive Select 2
29	30	Drive Select 3
31	32	Drive Select 4
33	34	Direction IN

Winchester Drive Power Cable





	Drive		Motherboard	
Pin	Signal	Wire Colour	Signal	Wire Colour
1	+12V	Yellow	+5V	Red
2	0V	Black/White	0V	Black
3	0V	Black	0V	Black/White
4	+5V	Red	+12V	Yellow

Electronic System 3

1. Outline Of Controller.
2. Integrated Circuit Catalogue
3. Mnemonics

1. Outline of Controller

Introduction

The Winchester disk drive controller is a single board expansion card which fits into either one of the system expansion slots and connected to the disk drive by a ribbon cable.

The board acts as the interface between the processing system and the Winchester disk drive.

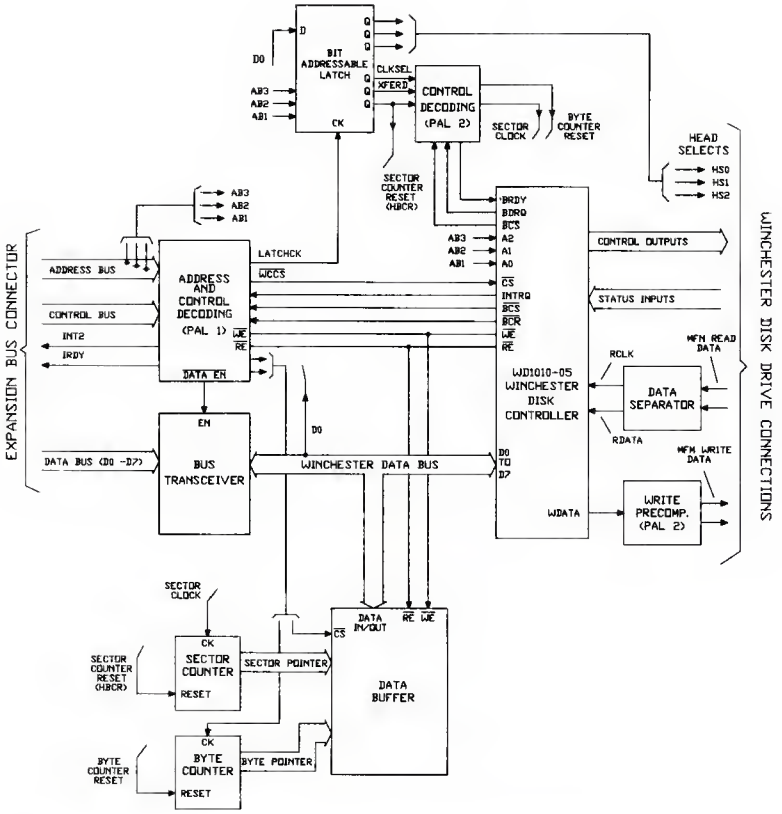
Description

The controller is broken into seven parts; the WD1010-05, Data seperator, write precompesation, addressing, RAM buffer control port and finally a data bus.

Winchester Disk Controller (WD1010-05)

The Winchester disk interface consists of a WD1010-05 and associated buffers.

The interface provides all the control functions necessary for formatting and transferring data to and from the winchester disk.



Winchester Controller Board Block Diagram

The WD1010-05 is selected by WCCS from PAL1.

Head select is controlled by the control port (IC8).

The controllers registers are selected by AB1 -3 from the Apricot.

Data Separator.

The DP8460 (IC2) data separator receives digital pulses from a differential line receiver which converts the data from balanced to TTL format. The data separators lock to the frequency of these input pulses and separates them into synchronized data and clock signals.

Write Precompensation

The Rodime RO350 does not require write precompensation although the controller is capable of producing early, normal and late data. Write data (WDATA) from the WD1010-05 can be used to drive a delay line, (Not normally fitted). This generates two extra write data signals delayed by 10ns and 20ns. These data signals are then selected by PAL2 which is controlled by RWC/EARLY and LATE from the WD1010-05.

The write data output of PAL2 is converted to balanced format by the differential line drive.

Addressing.

The PAL1 is used to interface the address bus from the Apricot to the Winchester controller. It receives address lines AB4-AB8 which allows the controller to detect accesses to the WD1010-05.

The control port and the data port AB0 qualifies the device selects and ALE is used to prevent glitches as the addresses change.

When the WD1010-05 isolates the local bus to perform a data transfer the PAL1 would produce NRAMCS from the appropriate address. PAL1 is also enabled by BCS from the WD1010-05.

The WD1010-05 interrupt request output (INTRQ) is bufferd by PAL1 and output as NINT2 to the Apricot.

To meet the address setup times of the WD 10 10-05, the read enable signal is delayed by qualifying it with the data enable signal whenever the controller is addressed by the Apricot IC8 also adds additional wait states by holding IRDY low until its Qc output goes high. This counter is clocked by the 5MHz clock (CLK5).

The expansion bus is buffered by tri-state drivers to avoid contention with other expansion cards.

Control Port

The control port (IC6) is an 8 bit addressable latch enabled by the signal latch-CK from PAL1.

The signals HS0-HS2 are used to select the winchester head.

CLKSEL defines if the system processor or the WD1010-05 causes the sector pointer to be incremented.

XFERD is a handshaking protocol informing the WD1010-05 that data is available.

HBCR is used to reset both the sector pointer and the byte pointer to zero. It is controlled by the system processor.

Data Bus

The local data bus is isolated from the expansion bus by IC5 an octal bus transceiver. Its direction is controlled by NIORC from the Apricot and enabled by NDATAEN from PAL1.

Static Ram.

This 8K x 8 or 2K x 8 bit buffer acts as a temporary store for all data transfers. Data is written into the buffer from the Apricot and then access is passed to the WD1010-05 which transferes the data to the winchester disk.

RAM chip select, read enable and write enable are controlled by PAL1.

The RAM addresses are generated by counters which form the byte pointer(IC7 +IC10) and sector pointer(IC8).

The byte counter is incremented by the byte clock from PAL 1 and goes high whenever RE or WE is active from either the CPU or WD10105.

The sector counter is clocked by sector CLK from PAL2. This is derived from either the Byte counter reaching its maximum count or from the buffer data request of the WD1010-05.

The byte counter is reset by the signal BCR from IC4. This is generated by either the system (HBCR) or the WD1010-05 (NWBCR).

The sector counter is only reset by the system (HBCR), this is to allow for a WD1010-05 option to be implemented.

Individual Bytes within the buffer cannot be specified by the system or WD1010-05.

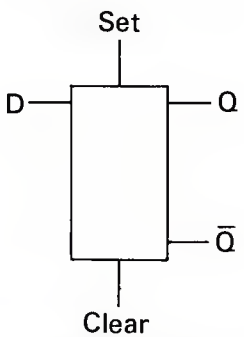
Byte counter specify a particular byte within a 512 byte section. The sector counter specifies a particular 512 bytes.

2. Integrated Circuit Catalogue

IC No.	Component	Description
1	WD1010-05	Winchester disk controller
2	DP8460-4	Data separator
3	PAL 20210	Program array logic
4	PAL 14H4	Program array logic
5	74LS245	Octal bus tranceiver
6	74LS259	8-bit addressable latch
7	74LS393	Dual 4 bit binary counter
8	74LS393	Dual 4 bit binary counter
9	26S02	Dual retriggerable monostable
10	74LS74	D-type edge triggered
11	74LS374	Octal D-type latch
12	74LS240	Octal buffered line driver/receiver
13	74LS240	Octal buffered line driver/receiver
14	HM6264P-15	8K x 8 static RAM
15	NOT FITTED	Delay line
16	SN75116	Differential line driver/receiver

IC	10

74S74 D-Type Flip-Flop

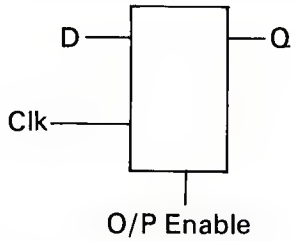


a) Produces the most significant bit of a 9 bit counter for the byte count.

b) Divides VCO by two to generate the read clock for the WD1010-05.

IC	11

74LS374 Octal D-Type Flip Flop.



Latches write data and precompensation outputs from the Write data and precompensation outputs from the Winchester controller. It also latches write clock and buffer data request.

IC	12, 13

74LS240 Octal Buffer Line Driver/Receiver

IC 12 Seven buffers are used to buffer controller signals to the Winchester disk drive. The remaining buffer is used as an input to a 4 bit binary counter for the sector clock.

IC 13. Buffers used to buffer Winchester controller signals from the Winchester disk drive.

IC	7, 8

74LS393 4 Bit Binary Counter

IC 7 dual 4 bit counter used to produce 8 bits of a 9 bit byte counter.

IC8 One counter used for the sector counter and the second allows for the addition of extra wait states.

IC	6

74LS259 8 Bit Addressable Latch

Select Inputs			Latch
C	B	A	Addressed
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

IC 6 Apricot address lines AB1-3 are decoded by this control port to give head select, HBCR, XFERD and CLKSEL.

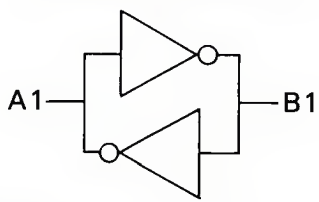
IC	9

AM26502 Dual Retriggerable Mono Stable.

Monostable triggered by read data will detect all 0's or 1's and produces DRUN. DRUN is used by the WD1010-05 to indicate pre-amble (all 0's)

IC	5

74 LS 245 Octal Bus Transeiver



Function Table		
Enable G	DIR	Operation
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Isolation

IC 5 Bi-directional buffer connecting expansion bus to Winchester controller bus enabled by DATEN.

IC	3, 4

Pal Programable Array Logic

Description of PAL.

The programmable array logic is used to reduce the number of discrete TTL components to allow the complex circuitry to fit onto a smaller area.

IC 3 PAL 1. The main function is address decoding from the Apricot.

IC 4 PAL 2. This PAL operates as a data selector to choose early data (EDATA), normal data (NDATA) and late data(LDATA) from the delay line. This is controlled by RWC/EARLY/LATE.

3. Mnemonics

Signal	Description	IC	Pin
Clk5	5MHz clock	PAL 1	B18
AB0	System address bus	PAL 1	
Ale	Address latch enable	PAL 1	5
IORC	Input output read command	PAL 1	2
DEN	Data enable	PAL 1	3
IOWC	Input write command	PAL 1	4
DB0-7	Data bus	IC5	2 3 4 5 6 7 8 9
DATAEN	Data enable	PAL 1	15
INTRQ	Interrupt request	PAL 1	1
WCCS	Winchester controller chip select	PAL 1	23
BSC	Buffered chip select	PAL 1	19
RAMCS	Ram chip select	PAL 1	18
Q2	Delayed read	PAL 1	13
RDY	Ready	PAL 1	17
IRDY	Input output ready	PAL 1	
WE	Write enable	PAL 1	21
INT2	Interrupt request 2 ext.	PAL 1	22
RE	Read enable	PAL 1	20
BYTECLK	Byte clock	PAL 1	16
LATCHCK	Latch clock	PAL 1	14
MR	Memory read	IC 1	5
CLKSEL	Clock select	PAL2	13
XFERD	Data transferred	PAL2	8
SECTOR CK (SCLK)	Sector clock	PAL2	14
BYTE CTR (BCR)	Byte counter	PAL2	15

Signal	Description	IC	Pin
RAMA8	Ram address 8	PAL2	12
RES	Master reset	IC1	5
WBCR	Winchester buffer count reset	PAL2	9
BRDY	Buffer ready	ICI	35
BDRQ	Buffer data request	IC1	36
STEP	Step	IC1	27
DIR	Buffer direction control	IC1	26
WG	Write gate	IC1	24
RWC	Reduced write current	IC1	33
INDEX	Index pulse	IC1	29
TK00	Track zero	IC1	31
READY	Ready disk	IC1	28
WF	Write fault	IC1	30
WC	Write clock	IC1	25
RCLK	Read clock	IC1	39
RDATA	Raw data	IC1	37
READ GATE	Read gate	IC1	38
DRUN	Data run	IC1	34
WDATA	Write data	IC1	21
LATE	Late (write precompensation)	IC1	22
EARLY	Early (write precompensation)	IC1	23
DS1	Drive select	PL2	
DS2-4	Drive select	PL2	28 30 32
HS0-2	Horizontal sync	PL2	14 18 4
WCLK	Write clock	PP3	4
MFMRD	Modified frequency modulated read data	IC2	20
MWD+/—	Modified frequency modulated write data	IC16	4+ 2—
VCO	Variable crystal oscillator	IC2	8
EDATA	Early data	PAL2	1
NDATA	Normal data	PAL2	2
LDATA	Late data	PAL2	3

4 Parts List

PCB Bill Of Materials For Apricot Winchester Controller
Options: Multiple sector transfers, 8Kx8 sector buffer, no write pre-compe

Part	Qty	Component
IC1	1	WD1010-05
IC2	1	DP8460-4
IC3	1	PAL20L10
IC4	1	PAL14H4
IC5	1	74LS245
IC6	1	74LS259
IC7	1	74LS393
IC8	1	74LS393
IC9	1	26S02
IC10	1	74274
IC11	1	74LS374
IC12	1	74LS240
IC13	1	74LS240
IC14	1	HM6264P-15 8Kx8 RAM 200nS or less
IC15	0	Not fitted on this version
IC16	1	SN75116 (Texas)
X01	1	10MHz crystal oscillator
RP1	1	8-pin SIL Res Pak 220/330R
RP2	1	8-pin SIL Res Pak 10K
RP3	1	8-pin SIL Res Pak 1K
R1	1	4K99 0.5% 0.125W H8
R2	1	100K 1% 0.25W MFR4
R3	1	1K5 1% 0.25W MFR4
R4	1	1K5 1% 0.25W MFR4
R5	1	4K7 1% 0.25W MFR4
R6	1	200R 1% 0.25W MFR4
R7	1	1K00 0.5% 0.125W
R8	1	47K 1% 0.25W MFR4
R9	1	1R 5%
R10	1	Not fitted to this version
RV1	0	Not fitted to this version
C1	1	47uF 10V electrolytic (axial)
C2	1	1uF 5% 63V MKS4
C3	1	0.1uF 5% 100V MKS4
C4	1	1.0nF 10% FKC2
C5	1	1.0nF 10% FKC2

Part	Qty	Component
C6	1	6.8nF 5% FKP2
C7	1	150pF 1% 630v Polystyrene
C8	1	100pF 1% 630V Polystyrene
C9	1	100pF 1% 630V Polystyrene
C10	0	Not fitted to this version
C11-C20	10	0.01uF Ceramic
J1	1	64-way DIN 41612 right-angle plug
A1	1	Apricot Winchester Disk Interface Part no. 111115-41
A2	1	Apricot Winchester Disk Power Cable Part no. 111118-41
A3	1	Paxolin cable protector Part no. 111119-61
	2	M2.5x14mm screws
	1	M2.5x6mm screw
	3	M2.5 nuts
	3	M2.5 shakeproof washers
	1	Disk Drive or Chassis Bad Sector

5 Circuit Diagrams

1. Winchester Controller CCT
2. Component Layout

Printed in England by Studio Press SP/0485/1M/AT